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REMARKS/ARGUMENTS

Claims 2-7, 10, 11, 13, 15, 16, and 18-26 and 31-33 are pending in this application. By this Amendment, Applicant amends claims 4-7, 10 and 20 and cancels claims 9, 12, 27-30, and 34-37.

Applicant greatly appreciates the Examiner's indication that claims 2-4, 6, 7, 13, 15, 16 and 18-22.

Claims 4, 5, 6, 7, 9, 10, 12, and 20 were objected to because in all the independent claims, Applicant recites a coil divided into inductors. The Examiner alleged that "it appears from the figures that there [are] four inductors connected in series instead of a single coil divided into four inductors." Applicant has amended claims 4-7, 10 and 20 and canceled claims 9 and 12 to correct the minor informalities noted by the Examiner. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the objection of claims 4, 5, 6, 7, 9, 10, 12, and 20.

Claims 5, 9, 10-12, 23, 24, 26, 27, 28, 30, 31, 33, 34, 35 and 37 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Senda et al. (U.S. 5,197,170) in view of Golant et al. (U.S. 3,879,690). And claims 5, 9-12 and 23-37 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Okubo (U.S. 5,583,470) in view of Golant et al. Applicant respectfully traverses these rejections.

Claims 9, 12, 27-30 and 34-37 have been canceled. Accordingly, Applicant respectfully submits that the prior art rejection of these claims is moot.

Claim 5 has been amended to recite:

"A delay line comprising:
at least four inductors; and
a laminated body including a plurality of insulating layers and at least four stages of low pass filters including said at least four inductors and a plurality of capacitors; wherein
one of the plurality of capacitors is connected to an end of at least one of the at least four inductors and is located on a first insulating layer, and another of the plurality of capacitors is

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**connected to another end of said at least one of the at least four inductors and is located on a second insulating layer; and
an insulating layer having said at least one of the at least four inductors is interposed between the first insulating layer and the second insulating layer."** (Emphasis added)

Claim 10 has been amended to recite:

"A delay line comprising:
at least four inductors; and
a laminated body including a plurality of insulating layers and at least four stages of low pass filters including said at least four inductors and a plurality of capacitors; wherein
the at least four inductors are defined by a plurality of coil conductor patterns arranged on the same plane of the insulating layers of the laminated body;
a portion comprising the coil conductor patterns is interposed between a first portion comprising at least one of the plurality of capacitors and a second portion comprising another of the plurality of capacitors; and
the insulating layers have a plurality of via holes for connecting the coil conductor patterns that define the at least four inductors." (Emphasis added)

The present claimed invention including "one of the plurality of capacitors is connected to an end of at least one of the at least four inductors and is located on a first insulating layer, and another of the plurality of capacitors is connected to another end of said at least one of the at least four inductors and is located on a second insulating layer," "an insulating layer having said at least one of the at least four inductors is interposed between the first insulating layer and the second insulating layer" and "a portion comprising the coil conductor patterns is interposed between a first portion comprising at least one of the plurality of capacitors and a second portion comprising another of the plurality of capacitors" minimizes stray capacitance between the capacitors, which achieves greatly improved characteristics of a group delay time of the delay line (see, for example, the last full paragraph on page 2 of the specification, as

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originally filed).

The Examiner alleged that Senda et al. and Okubo teach all of the features recited in claims 5 and 10, except for the inductors and the capacitor including at least four stages of a low pass filter. The Examiner further alleged that Golant et al. teaches inductors and a capacitor that make up stages of a filter. Thus, the Examiner concluded that it would have been obvious to connect the ends of the inductors of Senda et al. or Okubo in the circuit configuration of Golant et al. "in order to make a low pass filter."

However, none of Senda et al., Okubo and Golant et al. teach or suggest the specific combination and arrangement of elements recited in claims 5 and 10. Particularly, none of Senda et al., Okubo and Golant et al. teach or suggest "one of the plurality of capacitors is connected to an end of at least one of the at least four inductors and is located on a first insulating layer, and another of the plurality of capacitors is connected to another end of said at least one of the at least four inductors and is located on a second insulating layer" and "an insulating layer having said at least one of the at least four inductors is interposed between the first insulating layer and the second insulating layer" as recited in claim 5 of the present application or "a portion comprising the coil conductor patterns is interposed between a first portion comprising at least one of the plurality of capacitors and a second portion comprising another of the plurality of capacitors" as recited in claim 10 of the present application.

In contrast, as clearly seen in Figs. 3 and 5 of Senda et al., all of the inductors 16a, 16b of Senda et al. are disposed above the capacitors 6, and none of the inductors 16a, 16b are interposed between a first insulating layer having a capacitor disposed thereon and a second insulating layer having a capacitor disposed thereon. Thus, Senda et al. clearly fails to teach or suggest "one of the plurality of capacitors is connected to an end of at least one of the at least four inductors and is located on a first insulating layer, and another of the plurality of capacitors is connected to another end of

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said at least one of the at least four inductors and is located on a second insulating layer" and "an insulating layer having said at least one of the at least four inductors is interposed between the first insulating layer and the second insulating layer" as recited in claim 5 of the present application or "a portion comprising the coil conductor patterns is interposed between a first portion comprising at least one of the plurality of capacitors and a second portion comprising another of the plurality of capacitors" as recited in claim 10 of the present application.

Similarly, none of the inductors 21a and 21b of Okubo (see, for example Fig. 11 of Okubo) are interposed between a first insulating layer having a capacitor disposed thereon and the second insulating layer having a capacitor disposed thereon. In contrast, the capacitors 32 of Okubo are interposed between the insulating layers having the inductors 21a and 21b disposed thereon. Thus, Okubo clearly fails to teach or suggest "one of the plurality of capacitors is connected to an end of at least one of the at least four inductors and is located on a first insulating layer, and another of the plurality of capacitors is connected to another end of said at least one of the at least four inductors and is located on a second insulating layer" and "an insulating layer having said at least one of the at least four inductors is interposed between the first insulating layer and the second insulating layer" as recited in claim 5 of the present application or "a portion comprising the coil conductor patterns is interposed between a first portion comprising at least one of the plurality of capacitors and a second portion comprising another of the plurality of capacitors" as recited in claim 10 of the present application.

Golant et al. fails to teach or suggest any separate and distinct capacitors and inductors, and instead, teaches a conductive strip 51 disposed on the upper surface of a substrate 50 which produces an inductance and a capacitance. Golant et al. fails to teach or suggest any separate insulating layers having capacitors and inductors

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disposed thereon, and certainly fails to teach or suggest "one of the plurality of capacitors is connected to an end of at least one of the at least four inductors and is located on a first insulating layer, and another of the plurality of capacitors is connected to another end of said at least one of the at least four inductors and is located on a second insulating layer" and "an insulating layer having said at least one of the at least four inductors is interposed between the first insulating layer and the second insulating layer" as recited in claim 5 of the present application or "a portion comprising the coil conductor patterns is interposed between a first portion comprising at least one of the plurality of capacitors and a second portion comprising another of the plurality of capacitors" as recited in claim 10 of the present application.

Accordingly, Applicant respectfully submits that Senda et al., Okubo and Golant et al., applied alone or in combination, fail to teach or suggest the unique combination and arrangement of elements recited in claims 5 and 10 of the present application.

In view of the forgoing amendments and remarks, Applicant respectfully submits that claims 5 and 10 are allowable. Claims 11, 23-26 and 31-33 depend upon claims 5 and 10, respectively, and are therefore allowable for at least the reasons that claims 5 and 10 are allowable. In addition, claims 2-4, 6, 7, 13, 15, 16 and 18-22 are allowable as indicated by the Examiner.

In view of the foregoing amendments and remarks, Applicant respectfully submits that this application is in condition for allowance. Favorable consideration and prompt allowance are solicited.

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The Commissioner is authorized to charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1353.

Respectfully submitted,

Date: August 21, 2003


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